a first interconnect layer coupled between the programmable logic portion of the PLD and the embedded core, the first interconnect layer having a set of pitches selected from:

(i) the first vertical pitch and the second horizontal pitch; and

(ii) the first horizontal pitch and the second vertical pitch.

22. (New) The system of Claim 21, wherein the external memory circuit comprises one of a group of integrated circuits comprising: an EEPROM, an EPROM, and a PROM.

23. (New) The system of Claim 21, wherein the programmable logic portion of the PLD is a field programmable gate array (FPGA).

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24. (New) The system of Claim 21, wherein the embedded core is a microprocessor.

25. (New) The system of Claim 21, wherein the interconnect layer was routed using a routing program having as an input the set of pitches.

26. (New) The system of Claim 25, wherein the PLD comprises a second interconnect layer coupled between the programmable logic portion of the PLD and the embedded core.

27. (New) The system of Claim 26, wherein the set of pitches is divided for input to the routing program, wherein one pitch in the set of pitches is used for the first interconnect layer and the other pitch in the set of pitches is used for the second interconnect layer.

28. (New) The system of Claim 21, wherein the first horizontal pitch and the second horizontal pitch are also different.